IN THE CLAIMS

Amend Claims 61, 67, and 68 and add new Claims 69 - 128 so that the claims are as follows:

1 - 60. (Canceled)

61. (Currently amended) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region and occupying a lateral inversion area along the primary surface, the inversion area reaching a maximum value when the inversion layer is fully present, the varactor having a maximum capacitance dependent on the maximum inversion area in combination with the plate area, the plate electrode being at a plate-to-body voltage relative to the body electrode, the gate electrode being at a gate-to-body voltage relative to the body electrode, the inversion layer comprising multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign, each inversion portion appearing/disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero, each inversion portion meeting the plate region or/and being continuous with the another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion; and

adjusting the plate and maximum inversion areas to control the maximum and minimum capacitances of the varactor.

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62. (Original) A method as in Claim 61 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the plate and maximum inversion areas.

63. (Original) A method as in Claim 61 wherein the adjusting act involves adjusting the ratio of the maximum inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.

64. (Original) A method as in Claim 61 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

65. (Previously presented) A method as in Claim 61 wherein the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs.

66. (Original) A method as in Claim 61 wherein a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion situated below where a different corresponding one of the inversion portions occurs.

67. (Currently amended) A method as in Claim 61 wherein the gate electrode comprises multiple gate electrode portions of <u>doped</u> semiconductor material, each gate electrode portion situated above at least where a different corresponding one of the inversion portions occurs, each gate electrode portion being of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion.

68. (Currently amended) A method as in Claim 61 wherein:

the gate dielectric layer comprises a first gate dielectric portion and <u>a</u> second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs; and

the gate electrode comprises (a) a first gate electrode portion of <u>doped</u> semiconductor material of opposite conductivity type to the body region and (b) a second gate electrode portion of <u>doped</u> semiconductor material of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the

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second gate electrode portion situated above at least where a further corresponding one of the inversion portions occurs.

69. (New) A method as in Claim 65 wherein the gate dielectric portions comprise a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, the first gate dielectric portion extending between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region.

70. (New) A method as in Claim 69 wherein the gate dielectric portions include a third gate dielectric portion that extends to a location above the plate region.

71. (New) A method as in Claim 65 wherein each of at least two of the gate dielectric portions extend to a location above the plate region.

72. (New) A method as in Claim 66 wherein the surface depletion portions comprise a first surface depletion portion and a second surface depletion portion more heavily doped than the first surface depletion portion, the first surface depletion portion extending between the second surface depletion portion and the plate region such that the second surface depletion portion is spaced apart from the plate region.

73. (New) A method as in Claim 67 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

74. (New) A method as in Claim 67 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

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75. (New) A method as in Claim 74 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

76. (New) A method as in Claim 74 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

77. (New) A method as in Claim 68 wherein:

the first gate dielectric portion extends between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region; and

the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

78. (New) A method as in Claim 68 wherein the gate dielectric layer includes a third gate dielectric portion of approximately the same thickness as the first gate dielectric portion, the second gate electrode portion overlying the third gate dielectric portion.

79. (New) A method as in Claim 61 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

80. (New) A method as in Claim 79 wherein the gate electrode is situated outside the capacitance signal path.

81. (New) A method as in Claim 61 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

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82. (New) A method as in Claim 81 wherein the gate electrode is situated outside the inductance-capacitance signal path.

83. (New) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying an island area along the primary surface, the varactor having a maximum capacitance dependent on the island area, the gate dielectric layer comprising multiple gate dielectric portions which are of different respective thicknesses and which at least partially overlie the body region, each gate dielectric portion extending to a location above the plate region or/and being continuous with a gate dielectric portion thinner than that gate dielectric portion; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

84. (New) A method as in Claim 83 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

85. (New) A method as in Claim 83 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

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86. (New) A method as in Claim 83 wherein the gate dielectric portions comprise a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, the first gate dielectric portion extending between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region.

87. (New) A method as in Claim 83 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

88. (New) A method as in Claim 87 wherein the gate electrode is situated outside the capacitance signal path.

89. (New) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying an island area along the primary surface, the varactor having a maximum capacitance dependent on the island area, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion meeting the plate region or/and being continuous with a surface depletion portion more lightly doped than that surface depletion portion; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

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90. (New) A method as in Claim 89 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

91. (New) A method as in Claim 89 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

92. (New) A method as in Claim 89 wherein the surface depletion portions comprise a first surface depletion portion and a second surface depletion portion more heavily doped than the first surface depletion portion, the first surface depletion portion extending between the second surface depletion portion and the plate region such that the second surface depletion portion is spaced apart from the plate region.

93. (New) A method as in Claim 89 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

94. (New) A method as in Claim 93 wherein the gate electrode is situated outside the capacitance signal path.

95. (New) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying a lateral island area along the primary surface, the varactor having a maximum capacitance dependent on the island area, the gate electrode comprising multiple gate electrode portions which are of doped semiconductor material and which at least partially overlie the body region, each gate electrode portion being of different

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conductivity type or/and different average net dopant concentration than each other gate electrode portion; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

96. (New) A method as in Claim 95 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

97. (New) A method as in Claim 95 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

98. (New) A method as in Claim 95 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

99. (New) A method as in Claim 95 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

100. (New) A method as in Claim 99 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

101. (New) A method as in Claim 99 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

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102. (New) A method as in Claim 95 wherein:

the gate dielectric layer comprises (a) a first gate dielectric portion, (b) a second gate dielectric portion thicker than the first gate dielectric portion, and (c) a third gate dielectric portion; and

the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion overlying at least the third dielectric portion.

103. (New) A method as in Claim 102 wherein:

the first gate dielectric portion extends between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region; and

the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

104. (New) A method as in Claim 102 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

105. (New) A method as in Claim 95 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

106. (New) A method as in Claim 105 wherein the gate electrode is situated outside the capacitance signal path.

107. (New) A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and

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extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, the body region occupying a lateral body area along the primary surface, the varactor having a maximum capacitance dependent on the body area in combination with the plate area, the gate electrode comprising multiple gate electrode portions which are of doped semiconductor material and which at least partially overlie the body region, each gate electrode portion being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion; and

adjusting the plate and body areas to control the minimum and maximum capacitances of the varactor.

108. (New) A method as in Claim 107 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the plate and body areas.

109. (New) A method as in Claim 107 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

110. (New) A method as in Claim 107 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

111. (New) A method as in Claim 107 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

112. (New) A method as in Claim 111 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

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113. (New) A method as in Claim 111 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

114. (New) A method as in Claim 107 wherein:

the gate dielectric layer comprises (a) a first gate dielectric portion, (b) a second gate dielectric portion thicker than the first gate dielectric portion, and (c) a third gate dielectric portion; and

the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion overlying at least the third dielectric portion.

115. (New) A method as in Claim 107 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

116. (New) A method as in Claim 115 wherein the gate electrode is situated outside the capacitance signal path.

117. (New) A method comprising:

providing a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction;

applying (a) a plate-to-body voltage between the plate and body electrodes and (b) a gate-to-body voltage between the gate and body electrodes; and

varying the plate-to body voltage in a selected positive or negative direction while maintaining the gate-to-body voltage approximately constant at a selected non-zero value to cause multiple portions of an inversion layer to progressively appear in the body region below the gate electrode, the inversion portions respectively corresponding to different transition values of the plate-to-body voltage at the non-zero value of the gate-to-body voltage, each inversion portion appearing/disappearing approximately at the corresponding

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transition value of the plate-to-body voltage and being electrically connected to the plate region directly or/and through at least one other of the inversion portions.

118. (New) A method as in Claim 117 wherein the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions appears/disappears.

119. (New) A method as in Claim 117 wherein a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion situated below where a different corresponding one of the inversion portions appears/disappears.

120. (New) A method as in Claim 117 wherein the gate electrode comprises multiple gate electrode portions of doped semiconductor material, each gate electrode portion situated above at least where a different corresponding one of the inversion portions appears/disappears, each gate electrode portion being of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion.

121. (New) A method as in Claim 120 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

122. (New) A method as in Claim 120 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

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123. (New) A method as in Claim 122 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

124. (New) A method as in Claim 117 wherein:

the gate dielectric layer comprises a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions appears/disappears; and

the gate electrode comprises (a) a first gate electrode portion of doped semiconductor material of opposite conductivity type to the body region and (b) a second gate electrode portion of doped semiconductor material of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion situated above at least where a further corresponding one of the inversion portions appears/disappears.

125. (New) A method as in Claim 117 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

126. (New) A method as in Claim 125 wherein the gate electrode is situated outside the capacitance signal path.

127. (New) A method as in Claim 117 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

128. (New) A method as in Claim 127 wherein the gate electrode is situated outside the inductance-capacitance signal path.

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